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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,626	10/01/2003	Yunteng Huang	026-0030	7841

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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,626	HUANG ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-29 and 33-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-29 and 33-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's response to the restriction/election requirement without traverse filed on 11/26/04 has been received and entered in the case. The following is a detailed Office action of the elected group II, claims 1-29 and 33-44.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11-22, 33-35 and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,218,876, issued to Sung et al.

As per claim 11, Sung discloses a circuit (Fig. 2) comprising:

a first signal generation circuit (the combination of PLLs 52 and 54) for generating an output signal (the signal on line 300) having a frequency which is proportional to that of an input signal (the signal on line 100, column 6, line 56, i.e., the formula shows Fout is proportional to Fin), said first signal generation circuit comprising:

a first phase locked loop (PLL 52) circuit for generating an intermediate signal (the signal on the line from PLL 52 to PLL 54, column 4, line 6) having a frequency which is proportional to the input signal frequency (proportional because circuit 52 is a PLL); and

a second phase locked loop circuit (PLL 54) for generating the output signal (on line 300) having a frequency which is proportional to the intermediate signal frequency (proportional because circuit 54 is a PLL);

wherein, for a given input signal frequency and a given output signal frequency, the intermediate signal frequency is selectable from a plurality of available frequencies (because factors N1, M1 and K1 are programmable, column 4, lines 21-22).

As per claim 12, selecting the bandwidth of the first PLL lower than the second PLL does not result in a structural distinguishable between the claimed circuit and Sung's circuit because factors N1, M1 and K1 are selectable (programmable). Specifically, it is merely a result of selecting the values of factors N1, M1 and K1 in PLL 52 and factors N2, M2 and K2 in PLL 54.

As per claim 13, see column 4, lines 52-55. Also, deriving the input signal from any source to feed the circuit having the structure in claim 11 does not result in a structural distinguishable between the claimed circuit and Sung's circuit.

As per claim 14, the recited limitation is met because factors N1, M1 and K1 in PLL 52 are programmable (column 4, lines 21-22).

As per claims 15-17, see column 6, lines 53-56, column 7, line 2.

As per claims 18-21, because the values of factors N1, M1 and K1 in PLL 52 and factors N2, M2 and K2 in PLL 54 are programmable, the recited limitations are met.

As per claim 22, the recited limitation is merely an intended use of the circuit of claim 11. Therefore, no patentable weight is given.

As per claim 33, this claim is merely a method to operate a circuit having the structure discussed in claim 11. Because Sung teaches the circuit, he inherently teaches the recited method to operate.

As per claims 34-35, the recited steps are clearly disclosed in Fig. 2 where the first PLL is 52 and the second PLL is 54.

As per claim 37, the specific example described in column 5, lines 22-40 meets the recited limitation.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 23-29 and 38-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,218,876, issued to Sung et al.

As per claim 23, Sung discloses a circuit comprises a first signal generating circuit wherein the first signal generating circuit having a structure as discussed in claim 11 herein above. He further explicitly discloses the circuit is used, in one application, in a computer networking system (column 7, lines 19-22) wherein the computer networking system comprises a first data processing system 302 having a first signal generating circuit (Fig. 5, column 7, lines 11-35). Sung does not explicitly disclose a second signal generating circuit having the same structure as the first signal generating circuit is included in the circuit.

The examiner takes Official Notice the fact that a computer networking system comprises a plurality of data processing systems networked together wherein each data processing system needs a signal generating circuit is notoriously well-known.

It would have been obvious to one skilled in the art at the time of the invention was made to include a second signal generating circuit having the same structure as the first signal generating circuit, i.e., using two PLLs connected in series. The motivation and/or suggestion for doing so would be to simplify the PLL circuit design in the second signal generating circuit (column 5, lines 41-47).

As per claim 24, the recited limitation is discussed in claim 23.

As per claims 25-27, the combination discussed in claim 23 does not explicitly teach or suggest packing the first and second signal generation circuits in a single integrated circuit, or a single printed wiring board, or different printed wiring boards within one system enclosure as called for in these claims, respectively. However, packaging these circuits in a way suitable for a particular application is well within the level of one skilled in the art as ruled by the Court. It would have been obvious to one skilled in the art at the time of the invention was made to pack the first and second signal generation circuits in a single integrated circuit, or a single printed wiring board, or different printed wiring boards within one system enclosure. The motivation would be to optimize the space, providing reliable system in a particular application.

As per claims 28-29, these claims are rejected for the same reason noted in claim 13.

As per claims 38-42, these claims are rejected for the same reasons noted in claims 23 and 25-29, respectively.

As per claim 43, because the frequency of an output signal in a PLL is proportional to the frequency of an input signal, a PLL is seen as a clock multiplying circuit. Therefore, the recited clock multiplying circuit reads on PLL 52 or PLL 54 in each of the first and second signal generating circuits.

As per claim 44, the recited limitation is disclosed in column 4, lines 52-55.

4. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,218,876, issued to Sung et al. in view of US Patent No. 6,114,987, issued to Bjornholt.

Sung discloses a structure which is capable of selecting the bandwidth of the first and second PLLs as discussed in claim 12 herein above but he does not explicitly teach a step of selecting the bandwidth of the first PLL lower than the bandwidth of the second PLL as called for in the claim.

Bjornholt explicitly teaches selecting the bandwidth of the first PLL lower than the bandwidth of the second PLL (Fig. 2). He further explicitly discloses the advantage would be to improve the phase noise characteristics of the input signal source (column 2, lines 11-14).

It would have been obvious to one skilled in the art at the time of the invention was made to select the factors in the Sung's circuit to have the bandwidth of the first PLL lower than the bandwidth of the second PLL to obtain the advantage taught by Bjornholt as discussed herein above.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

1/7/05

Minh Nguyen
Primary Examiner
Art Unit 2816